

ABSTRACT

A split-gate transistor having high coupling for use in flash memory, EPROMs, and EEPROMs. The transistor has a U-shaped floating gate and a U-shaped control gate, thereby significantly increasing the surface area of the gates and increasing the voltage coupling ratio. The high coupling permits the operation voltage to be reduced while increasing operation speed, and the configuration of the transistor gates allows their use in high density arrays without sacrificing speed or degrading operations. A process for forming such transistors is also disclosed, wherein a polysilicon layer is deposited and then etched so that nitride and polysilicon spacers may be formed in between portions of polysilicon which are then etched to form floating gates. The nitride portion of the spacers is removed, and then the dielectric and control gate layers are formed on the floating gates to yield an array of split-gate transistors.